S/N 08/650,719

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jeffrey S. Mailloux et al.	Examiner: Hong Kim
Serial No.:	08/650,719	Group Art Unit: 2187
Filed:	May 20, 1996	Docket: 303.623US1
Title:	ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION	

RESPONSE UNDER 37 C.F.R. § 1.116

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Commissioner for Patents
P.O. Box 1450
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Sir:

This response is timely filed in reply to the Final Office Action mailed on May 13, 2003. Please consider the appended remarks rendered in **Appeal Brief Format**.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Micron Technology, Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no interferences known to Appellants, Appellants' legal representative, or the Assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter.

There are three appeals known to Appellants, Appellants' legal representative, or the assignee that may directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter. These related appeals are currently pending before the Board and concern U.S. Patent Application Serial Number 08/984,560 (Atty. Ref:303.623US2), U.S. Patent Application Serial Number 08/984,562 (Atty. Ref:303.623US3), and U.S. Patent Application Serial Number 08/984,701 (Atty. Ref:303.623US5). A fourth, related appeal was

also pending with respect to U.S. Patent Application Serial Number 08/984,561 (Atty. Ref:303.623US6). However, a Notice of Allowability indicating allowance of all claims has been mailed to the Appellants (Paper 32), and this matter is no longer before the Board.

3. STATUS OF THE CLAIMS

Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are currently pending, and the rejection of these claims is appealed. A clean copy of the pending claims is included as Appendix I.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Supplemental Response to the Second Final Office Action mailed to the Appellants on March 15, 2002, in which claim 7 was amended to correct a typographical error.

5. SUMMARY OF THE INVENTION

As described in the Appellants' specification at page 7, line 6 - page 8, line 13, and shown generally in figures 9-11, embodiments of the invention disclosed relate to a memory device that selectably operates in either burst or pipelined modes. In one embodiment, an asynchronously addressable storage device 100 (Application, FIG. 9) includes mode circuitry 121 configured to select between burst and pipelined modes, and circuitry 122 operable in either the burst mode or pipelined mode and configured to switch between the burst mode and the pipelined mode for operating the device 100 in either mode. (Application, Pg. 29, lines 5-25).

Some embodiments of the invention can switch between burst access and pipelined modes of operation without ceasing ("on the fly"). (Application, Pg. 33, lines 17-19). In the burst mode of operation, an externally-generated memory address stored in the circuitry 122 is used to select data within the device 100. A counter 149 included in the circuitry 122 increments the stored external address to internally generate addresses for subsequent accesses. In the pipelined mode of operation, the circuitry 122 uses only external addresses 115 to access data within the device 100. (Application, Pg. 29, lines 8-16). As address information passes through

the memory, it is operative in one operational area before moving into another operational area. However, once moved, another set of address information may enter the operational area exited, and accesses to memory may overlap without conflicting. (Application, Pg. 8, lines 1-5). In addition to the embodiments described, other embodiments of varying scope, including systems, methods, and storage devices, such as memory circuits are discussed. (Application, Pg. 33, line 23 - Pg. 40, line 19).

6. ISSUES PRESENTED FOR REVIEW

1) Whether claim 61 was properly rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

2) Whether claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 were properly rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,610,864, issued to Manning (hereinafter "Manning").

7. GROUPING OF CLAIMS

All claims are to be taken independent of each other and each stands alone for purposes of this appeal.

8. ARGUMENT

a) The Applicable Law

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed

invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

b) The Reference

Manning: teaches a memory device which can be accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address. (Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34). The possibility of applying a pipelined architecture is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50). However, no details of the structure of the architecture, how it is applied, or its operation, are given.

c) Discussion of the Rejections

***c.1* – The rejection under § 112**

Claim 61 was rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. It has also been requested that this feature be added to the drawings. Because a prima facie case of lack of written description has not been made, and because the

requisite information has indeed been disclosed in the Application as filed, the Appellants respectfully traverse this rejection.

It is asserted in the Office Action that the limitation "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation" was not described in the specification. However, this element is in fact described in the Application as filed.

The Appellants have made references in other responses to the following text in the Application: pg. 27, lines 1-11; pg. 38, lines 11-15; and pg. 39, lines 9-16. The attention of the Examiner is now also directed to pg. 33, lines 13-21 and pg. 38, lines 11-15 of the Application. In these passages it is noted that some embodiments enable "using an initial externally generated address followed by one or more internally generated addresses" as well as "switching between burst access ... and ... pipelined modes of operation without ceasing." Further, "... in column-based switching, switching between burst EDO and pipelined EDO modes is accomplished on successive /CAS cycles ... this type of switching may be accomplished on either read or write cycles, e.g., from a burst EDO read cycle to a pipelined EDO read cycle, and vice-versa, or from a burst EDO write cycle to a pipelined EDO write cycle and vice-versa." Finally, as noted on pg. 27, lines 5-11, "After a first /CAS signal 114 cycle in burst mode which uses the initial external values supplied for addresses XA0 and XA1, counter 149 increments those initial values and provides new internally generated addresses A0 and A1 by supplying count 0 signal 140 and count 1 signal 141 to respective A0 and A1 locations in temporary storage 119 through MUXs 125, 124. In this manner, internal addresses may be generated based on an initial external address."

It is respectfully noted that "An application need not contain a word-for-word description of the claimed invention to satisfy the written description requirement. ... All that is needed is that the application reasonably convey the claimed subject matter." See Patent *Prosecution: Practice and Procedure Before the U.S. Patent Office* by Irah H. Donner, pg. 738, 2002.

To make out a prima facie case of lack of written description, four elements must be shown:

1) The application does not reasonably describe or convey the concepts :
2) to one of ordinary skill in the art
3) at the time of filing the patent application
4) of the claimed invention.

It is respectfully noted that "[i]f even one of these elements of the prima facie case is not present, the rejection is improper and must be withdrawn." *Id.* Since "[t]he initial burden is on the PTO to establish that the now claimed subject matter is not described by the specification ...", the Office must show why this element is not sufficiently described in the application as to each element of the prima facie case. *Id.*, citing *Ex parte Anderson*, 21 USPQ 2d 1241 (B.P.A.I. 1991). Since such a showing has not been made, and since the element is indeed described in the written description as filed, it is respectfully requested that the rejection under 35 USC § 112, first paragraph, be reconsidered and withdrawn.

***c.2* – The rejection under § 102**

Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 were rejected under 35 USC § 102(e) as being anticipated by Manning. First, the Appellants do not admit that Manning is prior art and reserve the right to swear behind this reference in the future. Second, the Appellants respectfully submit that a case of anticipation under 35 U.S.C. § 102(e) has not been established because Manning does not disclose each and every element of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64. Therefore, the Applicants respectfully traverse this rejection under 35 USC § 102(e).

c.2.1. Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims.

Manning specifically fails to disclose "circuitry ... configured to switch between the pipelined mode and the burst mode" as claimed by the Applicants in claim 1. Similarly, Manning fails to disclose that the burst mode and the pipelined mode are "extended data out modes" (claims 2-4); or that the "pipelined/burst mode circuitry" includes: a "buffer for storing

an (external) address", a "counter for incrementing an address", "is coupled for receiving an external address", or "multiplexed devices for providing an internally generated address" (claims 5-9).

Further, Manning does not teach "selecting between" a "burst mode ... and" a "pipelined mode", or switching between such modes (claims 33-34, 46, 59-61); much less how addresses are supplied while selecting or switching modes (claim 35), or what type of switching environment may be used in burst and pipelined modes of operation (claims 48-49). Finally, Manning does not describe a system including a microprocessor and memory "selectively operable either in a burst mode or a pipelined mode", or a storage device/memory including circuitry "switchable between burst and pipeline modes of operation" (claims 50, and 63-64).

Several assertions were made which attribute support to various concepts allegedly disclosed by Manning in the Office Action. However, a careful reading of each citation reveals that the discussion of the asserted elements is incorrect. These assertions have been made with respect to:

Claims 2, 3 - Manning does not disclose that the pipelined mode is an EDO mode of operation (the two concepts are never discussed in conjunction with each other).

Claim 9 - Manning does not disclose mode selection circuitry which includes a multiplexed device (the components referenced in the Office Action are an address counter 26 and a column address decoder 30).

Claim 34 - Manning does not disclose *switching* between the pipelined mode and the burst mode (Manning merely refers to the possibility of using a pipelined *architecture*).

Claim 35 - Manning does not disclose selecting an external address along with *selecting* between a burst mode and a pipelined mode (since Manning never discloses selecting between burst and pipelined modes in the same device).

Claims 48, 49 - Manning does not disclose several switching environments in conjunction with burst and pipelined modes (Manning merely refers to the possibility of using a pipelined *architecture*).

Two more erroneous assertions are directed toward all pending claims. First, it is not true that one must "select pipeline mode" to "work in the pipeline architecture". The assertion is erroneous because the pipelined mode does not need to be selected if a device always operates in that mode. Second, in contrast to assertions tendered by the Office, the feature of switching between pipelined and burst mode operations in the same memory are included in each of the rejected claims, since each claim is directed toward a single device, accessing a single device, accessing different locations in a single device, or a single device included in a system.

c.2.2. Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Applicants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support *switching* or *selecting* between burst and pipelined modes of operation, as claimed in claims 1, 33, 34, 46, 50, 59, 60, 61, 63, and 64 (and in all claims that depend from them)?

Second, the Office has failed to produce a *prima facie* case of anticipation. While the assertion is made that Manning discloses "mode circuitry to select between a burst mode and a pipelined mode", and that the circuitry is "configurable to select between [the] two modes", the Applicants' representative, after a careful study of Manning, was unable to locate any such selection circuitry, nor any aspect of such circuitry which was configurable to select between burst and pipelined modes of operation.

Finally, the Office has admitted the deficiencies of Manning in a related matter with respect to several elements claimed by the Appellants in the instant Application. The attention of the Office is directed to the following assertions made by the Appellants in the appeal of U.S. Application Serial No. 08/984,561:

"Manning Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Manning Col. 7, lines 43-54 speaks to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, **Manning never discusses the ability to select or switch between burst and pipelined modes of operation...**" (emphasis added)

This language was approved by the Office in a subsequent Notice of Allowability (Paper 32) mailed to the Appellants on March 21, 2003. In this Notice, the Office states:

"The claims are allowable over the prior art of record because the claims are distinguished from the prior art of record for the reasons as set forth in the ... appeal filed on 12/27/02 and because an update of a search previously made does not detect the combined claimed elements as set forth in claims 1-23."

For example, allowed claim 72 of U.S. Application Serial No. 08/984,561 reads:

A method for switching between pipeline and burst modes of operation, comprising:

maintaining a first enabling signal in an active state, the first enabling signal being an address-strobe signal;

maintaining an external mode select signal to select a pipeline mode;

receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and

switching the mode of operation to a burst mode on successive cycles of the second enabling signal while maintaining the first enabling signal in the active state.

Thus, Manning simply does not disclose any method or device for switching between burst and pipelined modes of operation. What is discussed by Manning is not identical to the subject matter of various embodiments of the invention as required by the M.P.E.P., and the rejection is under § 102 is therefore improper. Further, an updated search has been conducted by the Examiner in the referenced related matter, and none of the art reveals the ability to switch or

select between burst and pipelined modes of operation. Therefore, reconsideration and allowance of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested.

c.3 Why the claims are separately patentable:

While the separate patentability of each claim has been discussed in the "Argument" section above, as allowed in the M.P.E.P. § 1206, the reasons are summarized here to ensure completeness and as a matter of convenience for the Board.

Independent claim 1 is directed toward an asynchronously-accessible storage device having "mode circuitry configured to switch between a burst mode and a pipelined mode" and "circuitry operable in either a burst mode or pipelined mode ... for operating the asynchronously-accessible storage device in either mode." Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 1, dependent claim 2 adds "the burst mode and the pipelined mode are extended data out modes of operation." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 3 adds "the pipelined mode is an extended data out mode." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 4 adds "the burst mode is an extended data out mode." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 5 adds "the pipelined ... mode circuitry includes a buffer ... for storing an address." Manning does not disclose this combination of elements, and no other claim (except claim 6) has this unique combination of elements. To the elements of dependent claim 5, dependent claim 6 adds "the pipelined ... mode circuitry includes at least one counter ... for incrementing the address." Manning does not

disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 1, dependent claim 7 adds "the pipelined ... mode circuitry is coupled for reading an external address." Manning does not disclose this combination of elements, and no other claim (except claims 8 and 9) has this unique combination of elements. To the elements of dependent claim 7, dependent claim 8 adds "the pipelined ... mode circuitry includes a buffer ... for storing the external address." To the elements of dependent claim 7, dependent claim 9 adds "the pipelined ... mode circuitry includes multiplexed devices for providing an internally generated address to the storage device." Manning does not disclose these combinations of elements, and no other claims have these unique combinations of elements.

Independent claim 33 is directed toward a method of accessing a storage device comprising "receiving a first address", "obtaining a second address", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode" and "asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address." Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 33, dependent claim 34 adds "switching between the burst mode and the pipelined mode." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 33, dependent claim 35 adds "the second address is an external address." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 46 is directed toward a method of accessing a storage device comprising "selecting a pipelined mode of operation", "providing a new external address for every access associated with asynchronously accessing the ... device while in the pipelined mode

of operation", and "switching modes to a burst mode of operation". Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

To the elements of independent claim 46, dependent claim 48 adds "the burst mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching." Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 46, dependent claim 49 adds "the pipelined mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 50 is directed toward a system including "a microprocessor" and "a memory coupled to the microprocessor, the memory selectively operable either in a burst mode or a pipelined mode, wherein the memory is an asynchronous dynamic random access memory". Manning does not disclose this combination of elements, and no other independent claim (or claims depending from them) has this unique combination of elements.

Independent claim 59 is directed toward a method of accessing a storage device comprising "receiving a burst/pipeline signal", "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode ... in response to the burst/pipeline signal", and "accessing a storage element ... in the selected mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 60 is directed toward a method of accessing a storage device comprising "receiving a burst/pipeline signal", "selecting between outputting information ... and inputting information", "selecting between an asynchronously-accessible burst mode and an

asynchronously-accessible pipelined mode ... in response to the burst/pipeline signal" and "asynchronously accessing a storage element ... in the selected mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 61 is directed toward a method of accessing a storage device comprising "selecting a pipeline mode of operation", "providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in a burst mode of operation", "switching modes to the burst mode of operation", and "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 63 is directed toward a storage device having "an array of memory cells" and "mode circuitry for receiving a burst/pipeline signal". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 64 is directed toward a memory circuit having "an array of memory cells" and "burst/pipeline selection circuitry for determining a burst or a pipeline mode of operation". Manning does not disclose this combination of elements, and no other claim has this unique combination of elements.

c.4 -- The double patenting rejection:

Claims 59 and 60 were provisionally rejected under the judicially created doctrine of double patenting over claim 36 of co-pending Application No. 08/984,563. Claim 61 was provisionally rejected under the judicially created doctrine of double patenting over claim 59 of co-pending Application No. 08/984,561.

Co-pending U.S. Patent Application Serial No. 08/984,563 has not yet received any final indication of allowed claims. The Applicants request that the claims of the instant patent application be allowed to issue without a Terminal Disclaimer, and that the issued claims of the

instant application be compared to the claims of the cited co-pending applications to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Applicants will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon closing prosecution on the merits for the co-pending applications, as needed, or in the alternative, upon receiving an indication of allowance for the relevant claims in the instant application.

Co-pending U.S. Patent Application Serial No. 08/984,561 has received a final indication of allowed claims. The Applicants request that claim 61 of the instant application be compared to issued claim 59 of the cited co-pending application to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Applicants will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon receiving an indication of allowance for claim 61 in the instant application.

9. SUMMARY

It is respectfully submitted that claim 61 is indeed supported by the subject matter contained in the Application as-filed, and that a case of anticipation under 35 U.S.C. §102 has not been established with respect to claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64. Therefore, reconsideration and withdrawal of the rejections of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 is respectfully requested.

The Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicants' attorney, **Mark Muller at (210) 308-5677**, or the undersigned attorney, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,
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